Abstract:
Designers of high-speed silicon chips have often had to compromise on performance levels for their integrated circuit designs because of physical weaknesses appearing during design verification or even in production. This has necessitated building redundancy into chip designs to allow for the imperfect environments of production and use that vary from the ideal of the design workbench. Issues such as voltage variations, thermal heat effects, electrostatic discharge, internal radiation and crosstalk can all downgrade the performance and reliability of a perfect design.

Working together to design robust silicon chips

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With circuit detail resolutions now descending to 65 and 45 nm, such problems are becoming ever more acute. All too often, chip designs pass traditional checks, yet fail when manufactured in silicon, forcing design teams to turn to costly diagnostic and repair methods or - worse still - throw the chip away.

Three major European semiconductor manufacturers - Infineon, NXP Semiconductors and STMicroelectronics - got together in ROBIN to define and deal with such problems early in the design phase, thus avoiding problems further down the development flow or in the production phase. They were joined by a laboratory with strong expertise in quantum physics and four electronic design automation (EDA) companies.

Favouring first silicon success

"Our most important target was to favour 'first silicon success' without affecting the performance of the circuits," explains project leader Philippe Garcin of STMicroelectronics, which started ROBIN. The other partners joined either because they had similar problems as in the case of Infineon and NXP, new solutions they intended to put on the open market in the case of the EDA companies or long-term solutions in mind as far as the research organisation was concerned.

The chipmaking partners formalised the problems, specified software tools, models and design flows with strong interoperability, and proposed complementary test cases. Together with the EDA partners, they built new solutions that are now available for exploitation in line with these specifications.

A key objective was to optimise the design approach to both existing 130 and 90 nm and future 65 and 45 nm technologies by defining the most efficient trade-offs between circuit robustness in terms of yield and reliability, and efficient use of technology affecting performance, density and power consumption. The challenge was to maintain or enhance existing performance levels, while improving design reliability and robustness.

Taking a bottom-up approach

"We took a bottom-up approach, from technology to chip level and then to system-in-package (SIP) level," says Garcin. "We examined a wide range of issues, from power and substrate effects through signal interference to manufacturing cost."

While applications require smaller voltages and higher frequencies, miniaturisation adds new risks of voltage distortions. To reduce design iterations and avoid unreliability or failures, ROBIN aimed to prevent these effects very early in the design flow. The project addressed signal corruption in power distribution and on the substrate, and took into account the effects of interconnect crosstalk and natural radiations.

The MEDEA+ project attained its goal of obtaining the best from available and emerging technologies by defining optimal trade-offs between circuit robustness in terms of yield and reliability, and efficient use of technology - performance, density and power consumption - down to 45 nm. For example, on inter-block couplings, ROBIN allowed a decrease of simulation time by factor of four in very critical radio-frequency circuits.

As support for the microelectronics industry, the ROBIN partners developed the basic concept for a unified chip/package data exchange (CPX) environment. The two industry standards - ESDA and JEDEC - used to measure electrostatic discharges were both evaluated and discussed. In the course of the project, the benefits of ROBIN were demonstrated in automotive, telecommunications and multimedia applications. Co-operation was highly successful within the different work groups.

Co-operation key to European success

As a result of ROBIN, partners' competitiveness was much improved, in particular for high reliability applications such as networking and medical. "Coming together within the MEDEA+ framework made an important difference," explains Garcin. "At the end of the project, among its 50 outcomes, about 80% were available for exploitation: the same results would not have been possible - either in terms of quantity or in terms of quantity - if the partners had worked alone.

"By aligning their requests, the industrial partners were able to prepare concerted specifications for their EDA tool providers. Thanks to the standards-based approach used in ROBIN, it is technically possible to share the results of the project across European industry - and the consortium is already taking the developments further in a new research project."

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